

WHAT IS CLAIMED IS:

- 1 1. A multiple-gate transistor comprising:
2 a semiconductor fin formed in a portion of a bulk semiconductor substrate;
3 a gate dielectric overlying a portion of the semiconductor fin;
4 a gate electrode overlying the gate dielectric, the gate electrode having a bottom surface;
5 and
6 a source region and a drain region formed in the semiconductor fin oppositely adjacent to
7 the gate electrode, the source region having a source-substrate junction, and the drain region
8 having a drain-substrate junction;
9 wherein the bottom surface of the gate electrode is lower than the source-substrate
10 junction or the drain-substrate junction.
- 1 2. The structure of claim 1 wherein the gate electrode comprises polycrystalline or
2 amorphous silicon.
- 1 3. The structure of claim 1 and further comprising a silicide region formed over the gate
2 electrode.
- 1 4. The structure of claim 1 wherein the gate electrode is formed from a polycrystalline
2 semiconductor.
- 1 5. The structure of claim 1 wherein the gate electrode is formed from a metallic nitride.
- 1 6. The structure of claim 1 wherein the gate electrode is formed from a metallic silicide.

- 1 7. The structure of claim 1 wherein the gate electrode is formed from a metal.
- 1 8. The structure of claim 1 wherein the gate electrode has a substantially planar top surface.
- 1 9. The structure of claim 1 and further comprising spacers on sides of the gate electrode.
- 1 10. The structure of claim 1 wherein the semiconductor fin comprises silicon.
- 1 11. The structure of claim 1 wherein the semiconductor fin comprises silicon and
2 germanium.
- 1 12. The structure of claim 1 wherein the semiconductor structure further comprises an
2 etchant mask overlying the semiconductor fin.
- 1 13. The structure of claim 1 wherein the semiconductor fin has a fin width that is larger at the
2 top of the semiconductor fin than at the bottom of the semiconductor fin.
- 1 14. The structure of claim 1 wherein the gate dielectric comprises silicon oxide.
- 1 15. The structure of claim 1 wherein the gate dielectric comprises silicon oxynitride.
- 1 16. The structure of claim 1 wherein the gate dielectric comprises a high permittivity
2 material.
- 1 17. The structure of claim 1 wherein the gate dielectric comprises a material selected from
2 the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride,
3 and zirconium oxide, and combinations thereof.

- 1 18. The structure of claim 1 wherein the gate dielectric comprises a material with a relative
2 permittivity greater than about 5.
- 1 19. The structure of claim 1 wherein the gate dielectric has a thickness of between about 3
2 and about 100 angstroms.
- 1 20. The structure of claim 1 wherein the multiple-gate transistor is a triple-gate transistor.
- 1 21. The structure of claim 1 wherein the multiple-gate transistor is a double-gate transistor.
- 1 22. The structure of claim 1 wherein the multiple-gate transistor is an omega-gate transistor.
- 1 23. The structure of claim 1 wherein the bottom surface of the gate electrode is lower than
2 the source-substrate junction and the drain-substrate junction by at least about 50 angstroms.

1 24. A method of forming a multiple-gate transistor, the method comprising:
2 providing a bulk semiconductor substrate;
3 forming a semiconductor fin in the bulk semiconductor substrate;
4 forming isolation regions on sides of the semiconductor fin;
5 forming a gate dielectric and a gate electrode on a portion of the semiconductor fin, the
6 gate electrode having a bottom surface; and
7 forming a source region and a drain region in the semiconductor fin, the source region
8 having a source-substrate junction and the drain region having a drain-substrate junction, the
9 source-substrate junction or drain-substrate junction being higher than the bottom surface of the
10 gate electrode.

1 25. The method of claim 24 wherein the source-substrate junction and the drain-substrate
2 junction is higher than the bottom surface of the gate electrode by at least 50 angstroms.

1 26. The method of claim 24 wherein forming a semiconductor fin comprises:
2 forming a mask over the bulk semiconductor substrate; and
3 etching exposed regions of the semiconductor substrate to form the semiconductor fin.

1 27. The method of claim 26 further comprising removing the mask.

1 28. The method of claim 27 wherein the mask comprises a photoresist.

1 29. The method of claim 27 wherein the mask comprises a material selected from the group
2 consisting of silicon oxide, silicon oxynitride, silicon nitride, and combinations thereof.

- 1 30. The method of claim 24 and further comprising strapping the source and drain regions
2 with a conductive material.
- 1 31. The method of claim 24 and further comprising forming spacers on sides of the gate
2 electrode.
- 1 32. The method of claim 24 and further comprising performing selective epitaxy on the
2 source and drain regions.
- 1 33. The method of claim 24 wherein the semiconductor fin comprises silicon.
- 1 34. The method of claim 24 wherein the semiconductor fin comprises silicon and
2 germanium.
- 1 35. The method of claim 24 wherein the gate dielectric comprises silicon oxide or silicon
2 oxynitride or silicon nitride.
- 1 36. The method of claim 24 wherein the gate dielectric comprises a high permittivity
2 material.
- 1 37. The method of claim 24 wherein the gate dielectric comprises a material selected from
2 the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride,
3 and zirconium oxide, and combinations thereof.
- 1 38. The method of claim 24 wherein the gate dielectric comprises a material with a relative
2 permittivity greater than about 5.

- 1 39. The method of claim 24 wherein the gate dielectric has a thickness of between about 3
2 and about 100 angstroms.
- 1 40. The method of claim 24 wherein the gate electrode comprises polycrystalline or
2 amorphous silicon.
- 1 41. The method of claim 24 wherein the gate electrode comprises poly-SiGe.
- 1 42. The method of claim 24 wherein the gate electrode comprises a metallic nitride.
- 1 43. The method of claim 24 wherein the gate electrode comprises a metallic silicide.
- 1 44. The method of claim 24 wherein the gate electrode comprises a metal.
- 1 45. The method of claim 24 wherein the multiple-gate transistor is a triple-gate transistor.
- 1 46. The method of claim 24 wherein the multiple-gate transistor is a double-gate transistor.
- 1 47. The method of claim 24 wherein the multiple-gate transistor is an omega-gate transistor.

1 48. A method of forming a semiconductor device, the method comprising:
2 providing a silicon substrate;
3 etching portions of the silicon substrate to form at least one semiconductor fin;
4 forming a gate dielectric layer over the semiconductor fin;
5 forming a gate electrode layer over the gate dielectric layer;
6 etching portions of the gate electrode layer to form a gate electrode, the gate electrode
7 overlying sidewalls and a top surface of the semiconductor fin;
8 forming a region of material adjacent portions of the semiconductor fin not underlying
9 the gate electrode such that a sidewall of the semiconductor fin extends above an upper surface
10 of the region of material; and
11 doping the sidewall of the semiconductor fin above the region of material.

1 49. The method of claim 48 wherein forming an isolation region comprises depositing an
2 oxide material.

1 50. The method of claim 48 and further comprising forming a masking material over the
2 silicon substrate and wherein the step of etching portions of the silicon substrate is performed in
3 alignment with the masking material.

1 51. The method of claim 50 and further comprising removing the masking material after the
2 semiconductor fin is formed.

1 52. The method of claim 50 wherein the gate dielectric layer and the gate electrode layer are
2 formed over the masking material.

- 1 53. The method of claim 48 wherein forming a region of material comprises depositing a
2 dielectric layer.
- 1 54. The method of claim 48 wherein forming a gate dielectric layer comprises forming a
2 layer of a material with a relative permittivity greater than about 5.
- 1 55. The method of claim 48 and further comprising forming an isolation region adjacent the
2 semiconductor fin.
- 1 56. The method of claim 48 and further comprising removing the region of material after
2 doping the sidewall.